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DIFFERENT ROLES AND DESIGNS OF HETERO-GATE DIELECTRIC IN SINGLE- AND DOUBLE-GATE TUNNEL FIELD-EFFECT TRANSISTORS

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Abstract

Hetero-gate dielectric (HGD) engineering not only suppresses the ambipolar current but also enhances the on-current of tunnel field-effect transistors (TFETs). Based on two-dimensional device simulations, we examined the roles and designs of hetero-gate dielectric structure in single- and double-gate TFETs. Proper comparisons and analyses show that the roles and designs of source-side dielectric heterojunctions are similar, whereas those of drain-side dielectric heterojunctions are extremely different in single- and double-gate TFETs. For both device structures, the optimal position of a source-side dielectric heterojunction does not depend on the ratio of low/high-k equivalent oxide thicknesses (EOTs). When increasing the EOT ratio, the on-current enhancement by an optimized source-side dielectric heterojunction is first increased (EOT ratio < 12) and then saturated (EOT ratio > 12). The role of a drain-side dielectric heterojunction in enhancing on-current is limited in double-gate TFETs (every EOT ratio), but significant in single-gate devices (EOT ratio < 12). For EOT ratios < 12, the optimal position of a drain-side dielectric heterojunction in double-gate TFETs is around 2-3 nm farther from the source compared to that in single-gate TFETs. For EOT ratios > 12, the optimal position of a drain-side dielectric heterojunction in double-gate TFETs is not dependent on the EOT ratio, unlike single-gate TFETs. Those differences are due to the difference in the depths of local potential wells in the two TFET structures.

Keywords: Band-to-band tunneling; Double-gate transistor; Hetero-gate dielectric; High-*k* gate-insulator; Tunnel FET.

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VAI TRÒ VÀ THIẾT KẾ KHÁC NHAU CỦA ĐIỆN MÔI CỰC CỔNG DỊ CẤU TRÚC TRONG CÁC TRANSISTOR HIỆU ỨNG TRƯỜNG XUYÊN HẦM ĐƠN VÀ LƯỠNG CỔNG

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Tóm tắt

Kỹ thuật điện môi cực cổng dị cấu trúc không chỉ giúp giảm dòng lưỡng cực mà còn làm tăng dòng mở của transistor trường xuyên hầm (tunnel field-effect transistr (TFET)). Dựa trên mô phỏng hai chiều, chúng tôi nghiên cứu vai trò và thiết kế của lớp điện môi dị cấu trúc trong TFET đơn và lưỡng cổng. Kết quả cho thấy vai trò và thiết kế của chuyển tiếp điện môi dị cấu trúc phía nguồn trong TFET đơn và lưỡng cổng hầu như giống nhau. Tuy nhiên, vai trò và thiết kế của chuyển tiếp điện môi dị cấu trúc phía máng rất khác nhau trong TFET đơn và lưỡng cổng. Trong cả hai cấu trúc, vị trí tối ưu của chuyển tiếp phía nguồn không phụ thuộc vào tỉ số bề dày ô-xít tương đương của các lớp điện môi có độ điện thẩm cao và thấp. Khi tăng tỉ số này, sự tăng dòng mở nhờ chuyển tiếp phía nguồn đầu tiên tăng (tỉ số < 12) và rồi bão hòa (tỉ số > 12). Đối với chuyển tiếp phía máng, vai trò của nó trong việc tăng dòng mở rất hạn chế trong TFET lưỡng cổng (mọi tỉ số) nhưng lại lớn trong TFET đơn cổng (tỉ số < 12). Khi tỉ số < 12, vị trí tối ưu của chuyển tiếp phía máng trong TFET lưỡng cổng xa cực nguồn hơn 2-3 nm so với trong TFET đơn cổng. Khi tỉ số > 12, vị trí tối ưu của chuyển tiếp phía máng trong TFET lưỡng cổng không phụ thuộc vào tỉ số này, nhưng trong TFET đơn cổng lại phụ thuộc. Những khác biệt trên là do các giếng thế định xứ trong hai cấu trúc có độ sâu khác nhau.

Từ khóa: Chất cách điện có độ điện thẩm cao; Điện môi cực cổng dị cấu trúc; FET xuyên hầm; Transistor lưỡng cổng; Xuyên hầm qua vùng cấm.

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1. INTRODUCTION

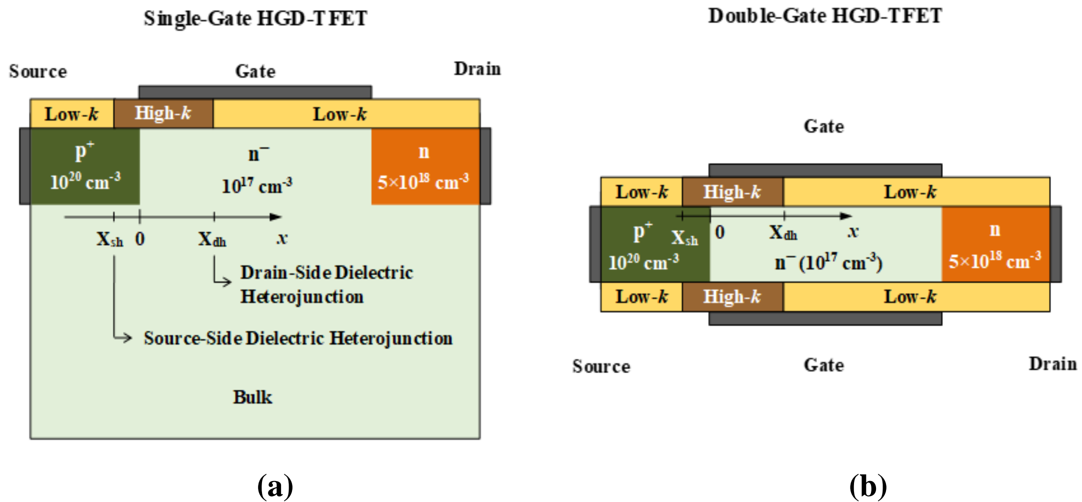
With the importance of mobile electronic devices in the modern world, low power consumption has been one of the most critical issues in integrated circuit technology. Scaling down the supply voltage is the most effective method to reduce the power consumption of electronic circuits. Although using metal-oxide-semiconductor field-effect transistors (MOSFETs) has shown great success for the past four decades, it also leads to a trade-off between operating speed and power dissipation in low voltage regimes (less than 1 V) (IEEE, 2020). This is because the subthreshold swing of MOSFETs' transfer characteristics is subjected to the physical limit of 60 mV/decade at room temperature due to the on-off mechanism based on the thermal injection of carriers (Sze, 1981). In order to overcome this inherent difficulty, tunnel field-effect transistors (TFETs) have been proposed (Appenzeller, Lin, Knoch, & Avouris, 2004; Wang et al., 2004). Because the on-off switching is determined by the mechanism of band-to-band tunneling (BTBT), TFETs can achieve a sub-60 mV/decade subthreshold swing to thoroughly resolve the trade-off between on- and off-currents (Choi, Park, Lee, & Liu, 2007; Seabaugh & Zhang, 2010).

Compared with conventional MOSFETs, TFETs have lower on-current (Koswatta, Lundstrom, & Nikonov, 2009) because it is more difficult to perform the BTBT than to implement the thermal diffusion process. Since the sub-60 mV/decade subthreshold swing of TFETs was experimentally demonstrated, a lot of methods have been proposed to improve the on-current (Chien & Vinh, 2013; Chien, Anh, Chen, & Shih, 2019; Liu et al., 2019; Nayfeh, Hoyt, & Antoniadis, 2009). Among them, material techniques are the most effective. For semiconductor materials, low-bandgap semiconductors (SiGe, InGaAs, etc.) were suggested for TFETs since the tunneling probability increases exponentially with decreasing bandgap (Chien & Vinh, 2013). For gate-insulator materials, high-*k* dielectrics (Al_2O_3, HfO_2, etc.) were applied to enhance the gate control on the channel and thus narrow the tunnel barrier at on-state (Boucart & Ionescu, 2007). However, detrimental ambipolarity is inherent in TFET devices. Unfortunately, low-bandgap semiconductors and high-*k* dielectrics all cause severe ambipolar currents (Mookerjea & Datta, 2008). Many techniques have been studied to suppress the ambipolar current of TFETs, such as lightly doped drain (Toh, Wang, Samudra, & Yeo, 2008), top/bottom configuration of gate/drain contacts (Hraziia, Amara, & Anghel, 2012), HGD structure (Xu, Cui, Sun, & Han, 2019), hetero dielectric box/pocket (Beniwal & Saini, 2019; Pandey, Dash, & Chaudhury, 2019), back-bias effect (Joshi, Singh, & Singh, 2020), vertically graded heterostructure of semiconductors (Lyu et al., 2020), channel sandwiched by drain (Bagga, Chauhan, Banchhor, Gupta, & Dasgupta, 2020), etc. Notably, HGD engineering is a special method since it not only suppresses ambipolar current but also enhances on-current.

The HGD technique has been widely applied in many kinds of TFETs to improve their on- and off-currents. However, most studies have used the HGD with the design parameters optimized for a typical TFET (single-gate, silicon, and fixed low/high-*k* EOTs). Our recent work has shown that the mechanisms of on-current enhancement by source- and drain-side dielectric heterojunctions are basically different (Shih, Chien,

Tran, & Chuan, 2020). Furthermore, HGD design depends on the EOT ratio of low- and high-*k* dielectrics, i.e., different low/high-*k* EOT ratios require different HGD designs to optimize the on-off switching of TFETs. Similar to the case of different EOT ratios, the different single- and double-gate structures also result in different gate-control capabilities. Therefore, it is predicted that the roles and designs of HGD in single- and double-gate TFETs are different, as will be shown in this paper. In order to do so, two-dimensional device simulations (Synopsys, 2013) are performed to model the electrical characteristics of TFETs. The paper consists of four sections, including the introduction and the conclusion. Section 2 describes the device structures and physical models used in the simulations. The roles of source- and drain-side dielectric heterojunctions are presented in Sections 3, respectively. The dependence of their design on the EOT ratio is then discussed in Section 4.

2. DEVICE STRUCTURES AND SIMULATION MODELS



(a) **(b)**

Figure 1. Schematic views of hetero-gate dielectric (HGD) TFETs with (a) single- and (b) double-gate structures

Figure 1 shows schematic views of hetero-gate dielectric TFETs having single- and double-gate structures. The body thickness of the double-gate TFETs was 10 nm to attain high gate coupling (Toh, Wang, Samudra, & Yeo, 2007) while still maintaining a negligible quantum confinement effect (Duan, Zhang, Wang, Li, Xu, & Hao, 2018). In both devices, the HGD structure with two dielectric heterojunctions was used for gate-insulator layers, which have a fixed physical thickness of 3 nm. For typical HGD-TFETs, a dielectric heterojunction consists of a low-*k* dielectric on one side and a high-*k* dielectric on the other side. In this investigation, SiO_2 (dielectric constant = 3.9) was adopted for low-*k* layers, whereas the dielectric constant of high-*k* layers was varied from 2.5 to 20 times higher than that of SiO_2. The two dielectric heterojunctions were positioned at the source and drain sides, which were determined by X_{sh} and X_{dh}, respectively. $In_{0.53}Ga_{0.47}As$, which is a direct bandgap semiconductor with a relatively small bandgap of 0.75 eV, was employed to attain high on-currents. The source region was heavily doped with an acceptor concentration of 10^{20} cm^{-3}. Small (10^{17} cm^{-3}) and medium (5×10^{18} cm^{-3})

donor concentrations were respectively specified in the channel and drain regions. Ideally abrupt doping junctions were assumed for properly determining the optimal positions of dielectric heterojunctions. To avoid any short-channel effect, a long length of 100 nm was designed for the channel region. A gate work function of 4.7 eV and a gate-to-source voltage of 0.6 V were applied in all simulations.

To evaluate the role of HGD as well as to examine the design of HGD in the TFETs, simulations of two-dimensional devices were carried out to model the electrical characteristics of TFETs, such as current-voltage curves and energy band diagrams. The tunneling current was taken into account in the simulations by generalizing the Shockley-Read-Hall recombination model to include free electron-hole pairs generated by the BTBT mechanism. The bandgap narrowing due to heavy doping and the Fermi-Dirac distribution were also included. Since $In_{0.53}Ga_{0.47}As$ is a direct bandgap semiconductor, Kane's direct BTBT model based on the nonlocal approach of the electric field at tunnel junctions was activated to compute the tunneling generation rate as (Kane, 1961):

$$G_{\mathrm{BTBT}} = A\frac{\xi^2}{E_g^{1/2}}\exp\left(-B\frac{E_g^{3/2}}{\xi}\right), \tag{1}$$

Where E_{g} is the effective bandgap of the semiconductor; ξ is the nonlocal electric field at the tunnel junctions; parameters A and B depend on the effective masses of electrons and holes:

$$A = \frac{gq^2 m_r^{1/2}}{36\pi\hbar^2}, \quad B = \frac{\pi m_r^{1/2}}{2\hbar q}, \tag{2}$$

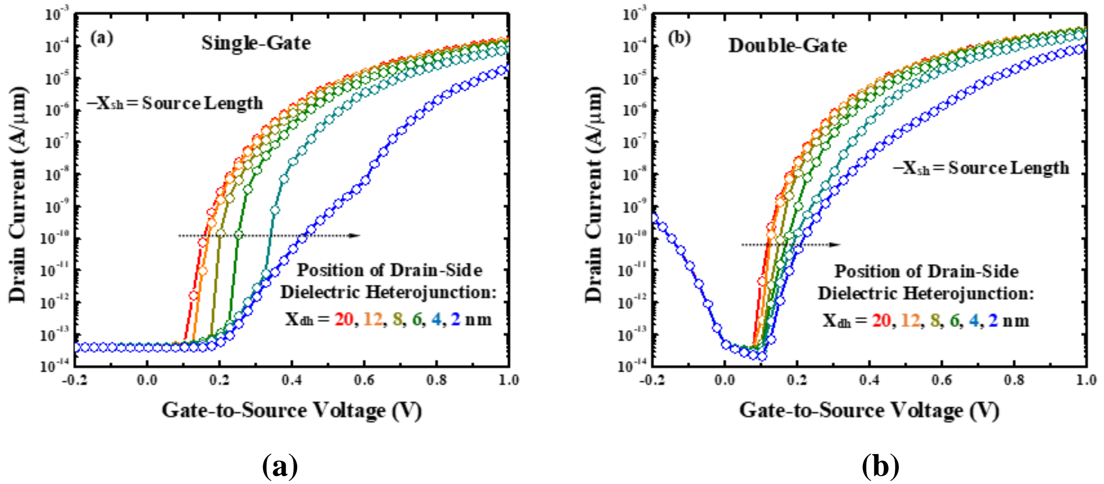
Where g is the degeneracy factor and m_r is the reduced mass, which is given by:

$$\frac{1}{m_r} = \frac{1}{m_e} + \frac{1}{m_h}. \tag{3}$$

Using the electron and hole effective masses (m_e and m_h, respectively) of $In_{0.53}Ga_{0.47}As$, A and B were easily calculated to obtain 1.4×10^{20} $\mathrm{eV}^{1/2}/\mathrm{cm.s.V}^2$ and 8.6×10^6 $\mathrm{V/cm.eV}^{3/2}$, respectively. Compared with experiment-based values ($1-1.4\times10^{20}$ $\mathrm{eV}^{1/2}/\mathrm{cm.s.V}^2$ and $8.3-9.2\times10^6$ $\mathrm{V/cm.eV}^{3/2}$, respectively) suggested by Smets et al. (2014), the calculated A and B are in good agreement with experiments.

3. RESULTS AND DISCUSSION

3.1. Role of drain-side dielectric heterojunction

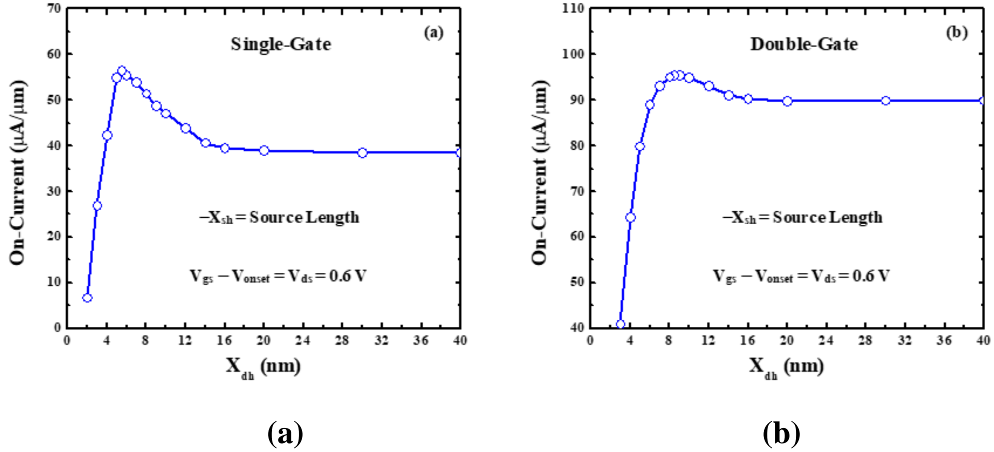


(a) **(b)**

Figure 2. Current-voltage transfer characteristics of (a) single- and (b) double-gate HGD-TFETs with various positions of drain-side dielectric heterojunction (X_{dh})

In order to examine the effects of a drain-side dielectric heterojunction on the electrical characteristics of TFETs, the current-voltage curves of single- and double-gate HGD-TFETs were plotted in Figure 2 for various heterojunction positions, X_{dh}. In this investigation, $-X_{sh}$ was set equal to the source length to definitely exclude the effect of a source-side dielectric heterojunction. A low/high-*k* EOT ratio of 10 was employed (i.e., the dielectric constant of high-*k* layers is 39) to maximize the on-current enhancement by the HGD engineering (Shih et al., 2020). Firstly, the ambipolar current is still observed in double-gate TFETs, although both the techniques of HGD and low drain doping are used simultaneously. For single-gate TFETs, the ambipolar current can be effectively suppressed by either the HGD or drain-doping engineering. Secondly, the hump effect, which separates high and low swing regions at hump voltage (V_{hump}), is clearly observed in single-gate TFETs with a short X_{dh} (< 6 nm). In double-gate TFETs, however, the hump effect is largely diminished, i.e., the separation of high and low swing regions is faint.

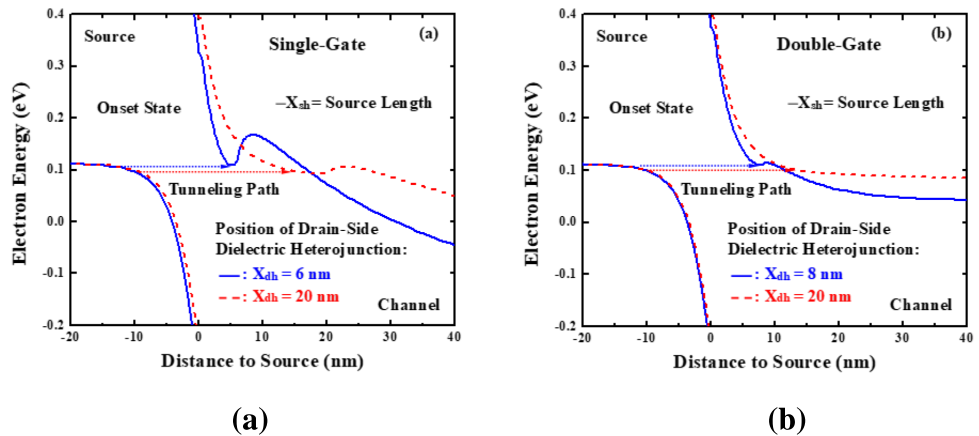
It should be noted that the on-current enhancement by a drain-side dielectric heterojunction originates indirectly from the decrease in average subthreshold swing. For the single-gate structure, the subthreshold swing first significantly decreases, then rapidly increases as X_{dh} drops from 20 nm to 2 nm. The hump effect limits the reduction of the subthreshold swing. This means that if the hump effect was suppressed by suppressing the current in the region of $V_{gs} < V_{hump}$, the subthreshold swing would decrease, and thus the on-current enhancement would increase. For the double-gate structure, the subthreshold swing first slightly decreases, then increases when X_{dh} drops from 20 nm to 2 nm. Although the hump effect is mitigated, it is not helpful in enhancing on-current because the mitigation of the hump effect is due to the increase of the current in the region of $V_{gs} < V_{hump}$.



(a) (b)

Figure 3. On-current of HGD-TFETs as a function of X_{dh} for (a) single- and (b) double-gate structures

To exactly evaluate the role of a drain-side dielectric heterojunction in enhancing the on-current of single- and double-gate TFETs, Figure 3 presents their on-currents as functions of X_{dh}. The on-current was determined as V_{gs} - V_{onset} = V_{ds}, where the onset voltage V_{onset} was defined as the V_{gs} when the drain current is 1 pA/μm. Generally, there exists a maximum on-current at a certain X_{dh} for either the single- or double-gate structure. Therefore, the drain-side dielectric heterojunction technique can be employed to ameliorate the on-current of both single- and double-gate TFETs. However, the on-current is enhanced much more in the single-gate than in the double-gate TFETs. Specifically, by properly designing the drain-side dielectric heterojunction, the on-current of the single-gate TFETs can be increased by 48%, whereas that of the double-gate counterparts can only be increased by 6%. In addition, the heterojunction positions that cause the on-currents to be maximized are also different in the single- and double-gate TFETs.



(a) (b)

Figure 4. Energy-band diagrams at onset state of (a) single- and (b) double-gate HGD-TFETs with different X_{dh}

Note: In this study, the onset votltage (V_{onset}) was defined as the gate voltage when the drain current is 1 pA/μm.

To optimize the on-current, the X_{dh} has to be 3 nm longer in the double-gate than in the single-gate TFET. The differences in the role and design of a drain-side dielectric heterojunction to optimize the on-current of single- and double-gate TFETs can be understood by analyzing their energy band diagrams at the onset state with different values of X_{dh}, as shown in Figure 4. As known from previous studies, the principal means to indirectly increase the on-current with a drain-side dielectric heterojunction is the formation of a local potential well at the tunnel junction. To form a local potential well, the drain-side dielectric heterojunction has to be close enough to the source-channel junction. It is seen that, although the local potential wells are formed, the well depth is much larger in the single- than in the double-gate TFET. The deeper the potential well, the more abrupt the transition of subthreshold tunnel width, and the smaller is the subthreshold swing. The potential well in the double-gate TFET is shallow because the strong coupling between the two gates reduces the role of high-*k* dielectric in modulating the channel potential. This also explains why it requires a longer X_{dh} (i.e., a longer high-*k* layer) to maximize the on-current in the double-gate than in the single-gate TFET.

3.2. Role of source-side dielectric heterojunction

In the off-state region, the drain-side dielectric heterojunction helps to suppress the ambipolar current of TFETs, whereas the source-side dielectric heterojunction has no impact on their off-state performance. In the on-state region, while the drain-side dielectric heterojunction indirectly affects the on-current by determining the subthreshold swing, the source-side dielectric heterojunction directly influences the on-current by modulating the on-state tunnel width (Shih et al., 2020). Therefore, the effect of device structure on the role of the source-side dielectric heterojunction is probably different from that on the role of the drain-side dielectric heterojunction.

The influence of a source-side dielectric heterojunction on the electrical characteristics of single- and double-gate TFETs can be clarified by analyzing their current-voltage curves with different heterojunction positions, X_{sh}, as presented in Figure 5. In this case, the drain-side dielectric heterojunction was set far away from the source-channel junction ($X_{dh} = 50$ nm) to avoid its effect on the on-state performance of TFETs. The drain-side dielectric heterojunction is still far enough from the drain-channel junction to effectively suppress the ambipolar current. For both structures, the on-current is maximized at $X_{sh} = 0$ and significantly decreased at $X_{sh} = -4$ and 4 nm. The degradation of on-current is larger for positive X_{sh} than for negative X_{sh}. For the negative side of X_{sh}, this is due to the strong coupling between the gate and source regions that reduces the electric field at the source-channel junction. For the positive side of X_{sh}, the on-current degradation is caused by the decreased gate control on the tunnel junction. Notably, the on-current degradations by the negative and positive shifts of the source-side dielectric heterojunction are almost the same in the single- and double-gate TFETs.

For a detailed consideration, Figure 6 plots the on-current against X_{sh} for the single- and double-gate TFETs. The variations of on-currents under the change of X_{sh} in the two TFET structures are similar, except that the on-current of the double-gate TFET is about two times higher than that of the single-gate device for every X_{sh}. The plots

definitely confirm that the on-currents of the two devices are maximized when the source-side dielectric heterojunction is exactly aligned with the source-channel junction. When moving the source-side dielectric heterojunction to the left from this optimal position, the on-currents first decrease rapidly and then reach saturation at $X_{sh} \sim -5$ nm. The on-currents of the HGD-TFETs at $X_{sh} < -5$ nm correspond to that of uniform high-*k* dielectric TFETs. Therefore, it is seen that the on-currents of single- and double-gate TFETs are enhanced by 125% and 100%, respectively, by using the optimally designed source-side dielectric heterojunction. For movements of the source-side dielectric heterojunction in the opposite direction, the on-currents decrease even more rapidly. Although not shown here, it is clear that the on-currents will be saturated at the current levels of the uniform low-*k* dielectric TFETs. Finally, it is found that the role of the source-side dielectric heterojunction is more important than that of the drain-side dielectric heterojunction in enhancing the on-current of TFETs, particularly in the double-gate structure.

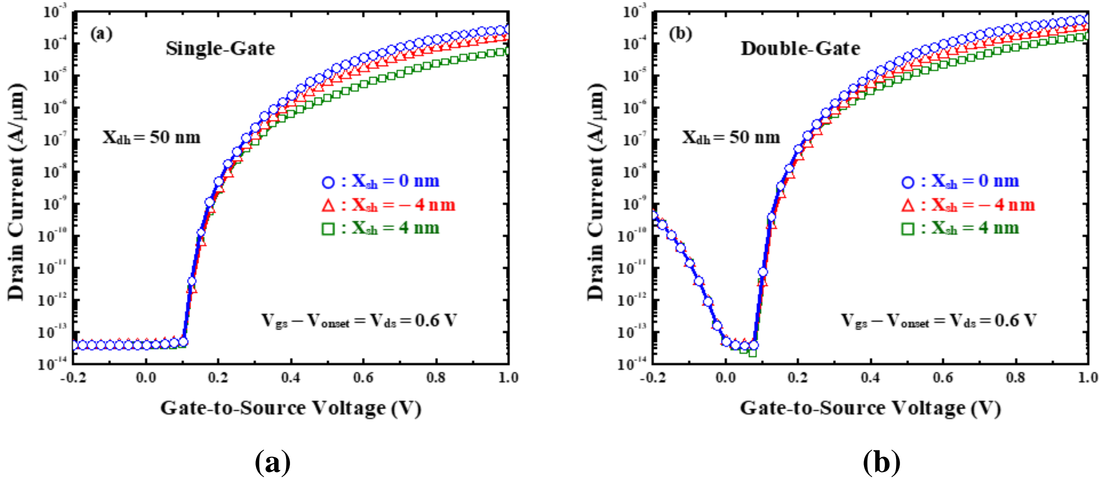


Figure 5. Input transfer characteristics of (a) single- and (b) double-gate HGD-TFETs with different positions of source-side dielectric heterojunction (X_{sh})

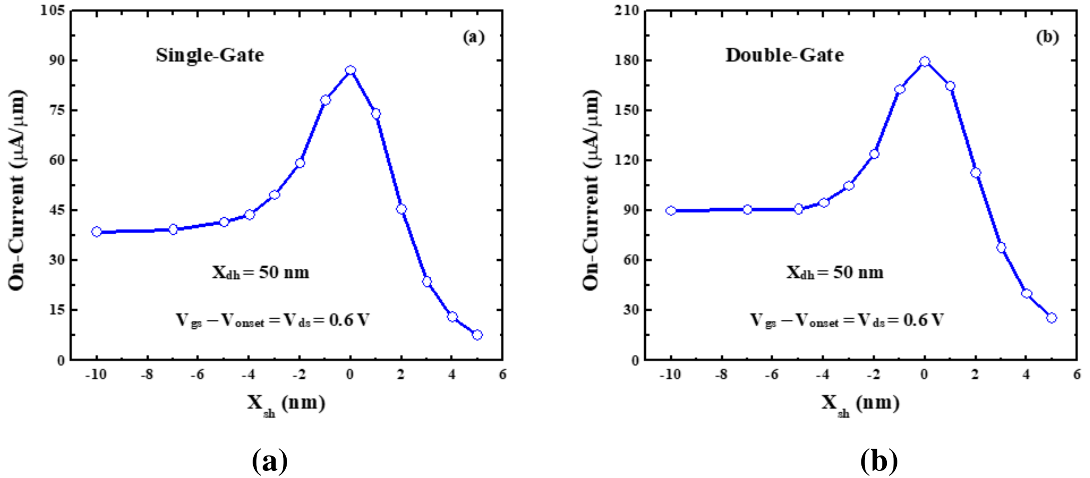
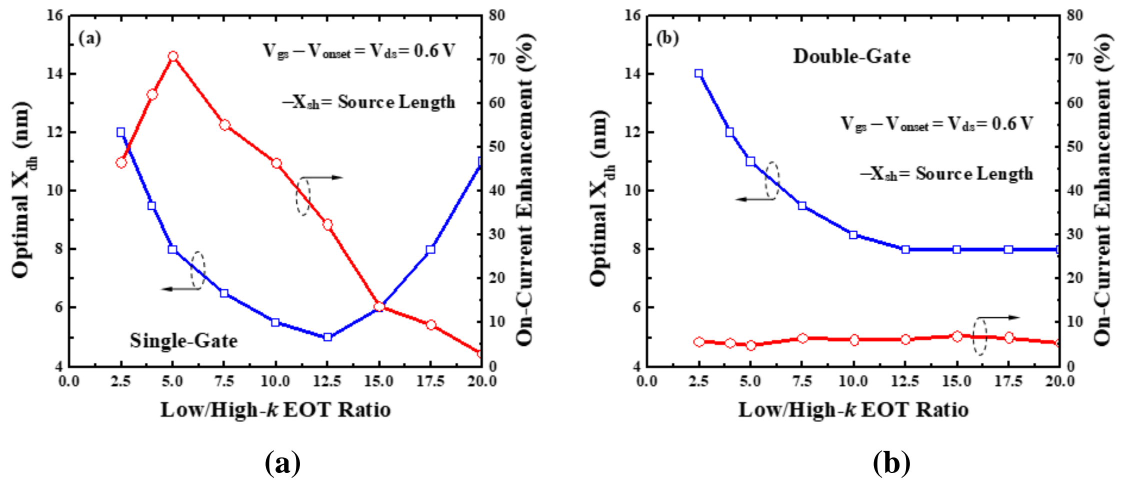


Figure 6. On-current as a function of X_{sh} in (a) single- and (b) double-gate HGD-TFETs

3.3. Dependence of HGD design on low/high-*k* EOT ratio

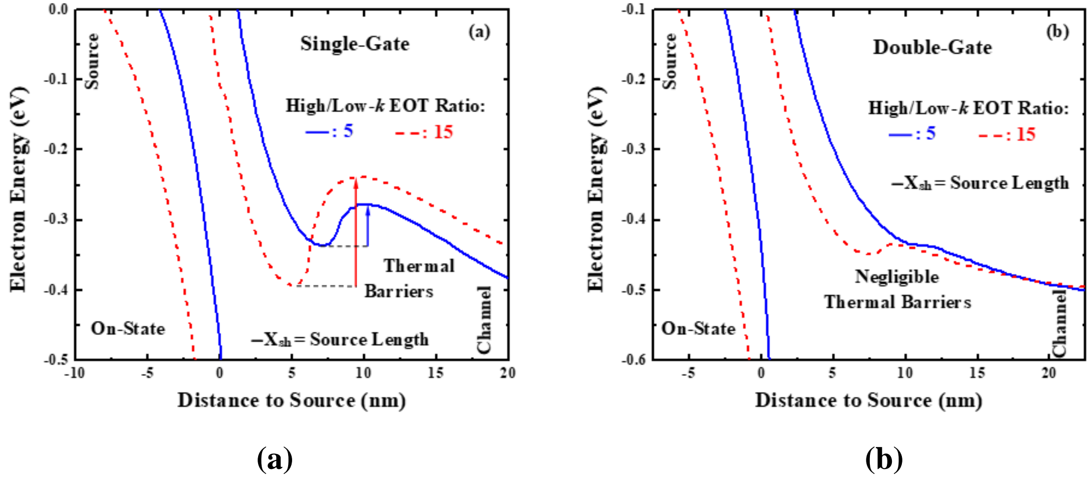
Previous sections examined and compared the roles of source- and drain-side dielectric heterojunctions in single- and double-gate TFETs. While the two device structures were presented in parallel for comparison, the two dielectric heterojunctions were separately investigated to draw proper conclusions on their roles in enhancing on-current. However, the low/high-*k* EOT ratio was fixed at 10. Because there are many high-*k* dielectric materials with a wide range of dielectric constants, and because scaling down EOT is a continuous trend in advanced CMOS technology, it is crucial to investigate the structural dependence of HGD design on the low/high-*k* EOT ratio. That investigation will be presented in this section.



(a) (b)

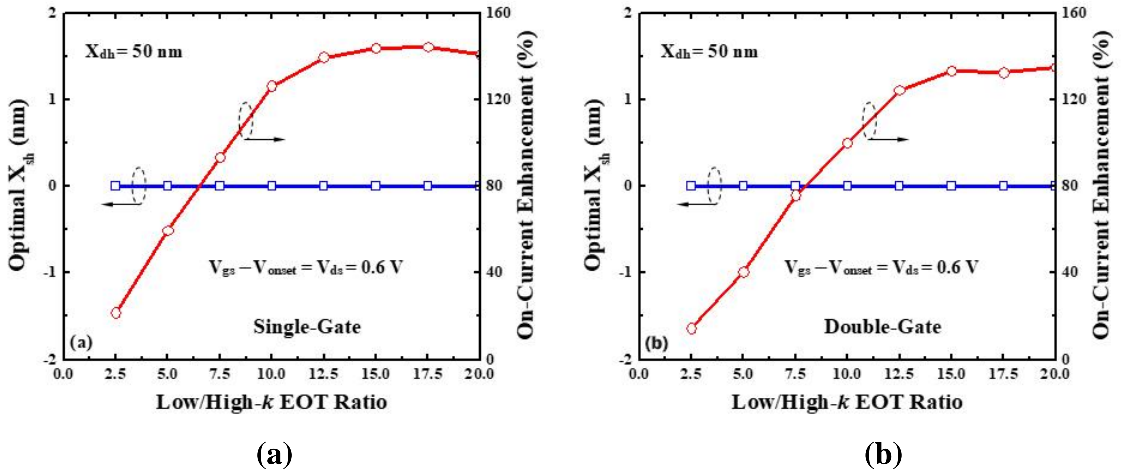
Figure 7. Optimal value of X_{dh} and on-current enhancement as functions of the low/high-*k* EOT ratio in (a) single- and (b) double-gate HGD-TFETs

Figure 7 shows the optimal position of a drain-side dielectric heterojunction as a function of low/high-*k* EOT ratio in single- and double-gate TFETs. The heterojunction position at which the on-current is maximized is considered to be optimal. At small ratios (< 12.5), the optimal X_{dh} in both single- and double-gate TFETs decreases with an increase in the ratio. This is because the increase of tunneling current at $V_{gs} > V_{hump}$ makes the exploitation of the decrease in subthreshold swing more effective. At large ratios (> 12.5), the optimal X_{dh} in single-gate TFETs increases with an increase in the ratio, whereas in double-gate TFETs the optimal X_{dh} is unchanged because of the saturation of the onset subthreshold swing. To examine the dependence of the role of the drain-side dielectric heterojunction on the EOT ratio, Figure 7 also displays the on-current enhancement as a function of low/high-*k* EOT ratio. The on-current enhancement is defined as the ratio of the incremental on-current due to applying the optimized drain-side dielectric heterojunction and the initial on-current of the uniform high-*k* dielectric TFET. For the single-gate structure, the on-current enhancement first increases (EOT ratio < 5) and then regularly decreases (EOT ratio > 5) down to nearly zero at the ratio of 20. For the double-gate structure, the on-current enhancement is almost unchanged with the change of the EOT ratio. For EOT ratios less than 15, the on-current enhancement is much smaller in the double-gate than in the single-gate TFET.



(a) **(b)**

Figure 8. Energy-band diagrams at on-state of (a) single- and (b) double-gate HGD-TFETs with different ratios of low/high-*k* EOTs



(a) **(b)**

Figure 9. Optimal value of X_{sh} and on-current enhancement as functions of the low/high-*k* EOT ratio in (a) single- and (b) double-gate HGD-TFETs

The difference in the roles of drain-side dielectric heterojunctions in single- and double-gate TFETs can be understood by comparing their energy band diagrams at on-state, as shown in Figure 8. It is easy to observe large differences in the depth of the local potential wells as well as their depth variation with the change of the EOT ratio. For the single-gate structure, the depth of the potential wells is large and increases with an increase in the EOT ratio. The existence of a potential well at the tunnel junction helps to reduce the subthreshold swing, but it also creates a thermal barrier to obstruct the movement of free electrons from the tunnel junction to the drain. When the EOT ratio is small, the former mechanism is dominant, which increases the on-current enhancement. When the EOT ratio is large, however, the latter mechanism is dominant, which decreases the on-current enhancement. For the double-gate structure, the potential well is very shallow, and its depth slightly increases with an increase in the EOT ratio. The on-current enhancement in double-gate TFETs is understandable if it is noted that the potential well

has a role in reducing the subthreshold swing and thus indirectly increasing the on-current.

The design of a source-side dielectric heterojunction depends on the EOT ratio in single- and double-gate TFETs, as shown in Figure 9. The optimal position of a source-side dielectric heterojunction is always aligned with the source-channel junction ($X_{sh} = 0$), irrespective of the device structure and the EOT ratio. The purpose of both these factors is to bend the energy band diagrams at the tunnel junction. Thus, an exact alignment of the dielectric heterojunction and the doping junction results in a resonance in narrowing the tunnel barrier to minimize the tunnel width most effectively. The figure also indicates that the roles of a source-side dielectric heterojunction in single- and double-gate TFETs are similar. For both TFET structures, the on-current enhancement rapidly increases with an increase in the EOT ratio, and it is saturated when the EOT ratio is greater than 12. The saturation of on-current enhancement occurs because the reduction of gate-source coupling by a source-side dielectric heterojunction has a lesser role in reducing the tunnel width at large EOT ratios.

4. CONCLUSION

Technology Computer-Aided Design simulation was used to explore the differences in the roles and designs of source- and drain-side dielectric heterojunctions in single- and double-gate TFETs. The role and design of source-side dielectric heterojunctions are almost independent of device structure. However, the suppression of the local potential well in double-gate TFETs, due to the high double-gate coupling, causes significant differences between the two TFET structures in the role and design of drain-side dielectric heterojunctions. Since double-gate, or more generally multi-gate architecture, is being employed increasingly in advanced CMOS technology, this study provides important guidelines for designing and applying HGD in TFET devices.

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